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14 Number of Pages (including this page)

Date: November 3, 2005
To: Matthew T. Henning - 2131
Location: United States Patent and Trademark Office
Fax No.: (571) 273-8300
From: James L. Clingan, Jr. - 30,163
Subject: 09/725,821- James D. Dworkin et al

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EXAMINER: Matthew T. Henning
GROUP ART UNIT: 2131
SERIAL NO.: 09/725,821
FILED: NOVEMBER 29, 2000
Inventor: James D. Dworkin et al

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DURATION: 30/10/1520

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ADDITIONAL FEES <table style="width:100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left;">Large Entity</th> <th style="text-align: left;">Small Entity</th> <th style="text-align: left;">Large Entity</th> <th style="text-align: left;">Small Entity</th> <th style="text-align: left;">Fee Description</th> </tr> <tr> <th>Fee Code</th> <th>Fee (\$)</th> <th>Fee Code</th> <th>Fee (\$)</th> <th></th> </tr> </thead> <tbody> <tr><td>1051</td><td>130</td><td>2051</td><td>65</td><td>Surcharge - late filing fee or oath</td></tr> <tr><td>1052</td><td>60</td><td>2052</td><td>25</td><td>Surcharge - late Provisional filing</td></tr> <tr><td>1053</td><td>130</td><td>1053</td><td>130</td><td>Non-English specification</td></tr> <tr><td>1812</td><td>2520</td><td>1812</td><td>2520</td><td>For filing a request for ex parte Reexamination</td></tr> <tr><td>1804</td><td>920*</td><td>1804</td><td>920*</td><td>Requesting publication of SIR prior to Examiner action</td></tr> <tr><td>1805</td><td>1840*</td><td>1805</td><td>1840*</td><td>Requesting publication of SIR after Examiner action</td></tr> <tr><td>1251</td><td>120</td><td>2251</td><td>55</td><td>Extension for reply within first month</td></tr> <tr><td>1252</td><td>450</td><td>2252</td><td>215</td><td>Extension for reply within second month</td></tr> <tr><td>1253</td><td>1020</td><td>2253</td><td>490</td><td>Extension for reply within third month</td></tr> <tr><td>1254</td><td>1590</td><td>2254</td><td>765</td><td>Extension for reply within fourth month</td></tr> <tr><td>1255</td><td>2160</td><td>2255</td><td>1040</td><td>Extension for reply within fifth month</td></tr> <tr><td>1401</td><td>500</td><td>2401</td><td>170</td><td>Notice of Appeal</td></tr> <tr><td>1402</td><td>500</td><td>2402</td><td>170</td><td>Filing a brief in support of an appeal</td></tr> <tr><td>1403</td><td>1000</td><td>2403</td><td>150</td><td>Request for oral hearing</td></tr> <tr><td>1451</td><td>1510</td><td>1451</td><td>1510</td><td>Petition to institute a public use proceeding</td></tr> <tr><td>1452</td><td>500</td><td>2452</td><td>55</td><td>Petition to revive - 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NOV 03 2005

In re Application of:
James D. Dworkin, et al.
Serial No.: 09/725,821
Filed: November 29, 2002
For: A CIRCUIT FOR GENERATING
HASH VALUES

November 3, 2005

Art Unit: 2131
Examiner: Matthew T. Henning
Docket No.: SC11015ZP

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REPLY BRIEF

COMMISSIONER FOR PATENTS
ALEXANDRIA, VA 22313
BOARD OF PATENT APPEALS & INTERFERENCES:

This reply brief is filed in the matter of the Appeal to the Board of Appeals and
Interferences of the rejection of the claims of the above-referenced application for patent.

11/04/2005 HDEMESS1 00000019 503079 09725821

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STATUS OF CLAIMS

Claims 1-8 and 14-18 are pending. Claims 9-13 have been canceled.

Claims 1-7, 14, 15, 17, and 18 stand rejected under 35 U.S.C. 103(a) as being obvious in view of Ober et al., U.S. Patent No. 6,708,273 (Ober); Childs, U.S. Patent No. 5,623,545 (Childs); Bruce Schneier, Applied Cryptography (Schneier); Turner et al., U.S. Patent No. 4,896,296 (Turner); and Batchner, U.S. Patent No. 4,314,349 (Batchner). Claim 8 stands rejected under 35 U.S.C. 103 (a) as being obvious in view of Ober, Childs, Schneier, Turner, Batchner and Niehaus et al., U.S. Patent No. 4,399,517 (Niehaus). Claim 16 stands rejected under 35 U.S.C. 103 as being obvious in view of Ober, Childs, Schneier, Turner, Batchner, and Masaki, U.S. Patent No. 4,739,195 (Masaki).

The rejection of claims 1-8 and 14-18 is being appealed.

GROUND FOR REJECTION TO BE REVIEWED ON APPEAL

1) Are claims 1-7, 14, 15, and 18 obvious under 35 U.S.C. 103(a) in view of Ober et al., U.S. Patent No. 6,708,273 (Ober); Childs, U.S. Patent No. 5,623,545 (Childs); Bruce Schneier, Applied Cryptography (Schneier); Turner et al., U.S. Patent No. 4,896,296 (Turner); and Batcher, U.S. Patent No. 4,314,349 (Batcher)? Is claim 8 obvious under 35 U.S.C. 103 (a) in view of Ober, Childs, Schneier, Turner, Batcher and Niehaus et al., U.S. Patent No. 4,399,517 (Niehaus)?

2) Is claim 16 obvious under 35 U.S.C. 103 in view of Ober, Childs, Schneier, Turner, Batcher, and Masaki, U.S. Patent No. 4,739,195 (Masaki)?

3) Is dependent claim 17 obvious under 35 U.S.C. 103 in view of Ober, Childs, Schneier, Turner, and Batcher.

ARGUMENT

The Examiner raised new points of argument in Grounds 1 and 3 to which applicants respond as follows:

GROUND 1

The Examiner pointed out that not all of the elements of FIG. 1 of applicants application are present in claim 1. Applicants point out, however, that it appears that the Examiner would consider FIG. 1 obvious based on his view of what one of ordinary skill in the art would do with the references used by the Examiner in rejecting claim 1 and dependent claims 2-7. Applicant's believe it is instructive to look at the references taken together and comparing them to applicants' FIG. 1.

GROUND 3

The Examiner argued that the applicants did not actually claim in claim 17, which depends on claim 15, that the register arrays were shared for both the SHA-1 and MD5 functions. Perhaps that is technically true but even assuming arguendo that it is true it is a distinction without a meaningful difference. The register array, as claimed, has one claimed characteristic for one function (claim 15) and a different characteristic for the other function (claim 17). The Examiner pointed out that Ober has a single register array. The Examiner did not, apparently because it was not possible to do so, argue that the register array of Ober met either of the characteristics as claimed. Accordingly, applicants do not see much merit to this position except to say that registers can be used for a lot of different things. The Examiner then argued that the register array of Childs provides both claimed characteristics. Even if true, this is insufficient because Childs performs only one of the claimed functions. Thus claim 15 and claim 17 cannot both be met by the register array of Childs. Accordingly, applicants submit that there is not a sufficient showing in the prior art for the notion of the register array providing both claimed characteristics and also being operational during both functions.

CONCLUSION

For at least the reasons set forth above and in the appeal brief, Applicants respectfully submit that the claims of the present application are allowable over the art cited during prosecution.

Respectfully submitted,



James L. Clingan, Jr.
Attorney for Appellants
Reg. No. 30,163
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Claims Appendix

1. An apparatus for selectively processing first and second cryptographic hash algorithms, comprising:

a register file (12) having at least five registers for storing chaining variables;

a function circuit (22) receiving first (B), second (C) and third (D) chaining variables and an output that provides a logical data value;

a first multiplexer (24) having an input coupled to the register file for receiving a fourth (E) chaining variable and an output that provides the fourth chaining variable when the first cryptographic hash algorithm is being processed by the apparatus and a zero value when the second cryptographic hash algorithm is being processed by the apparatus; and

a summing circuit (30) having a first input coupled to the output of the function circuit for receiving the logical data value, a second input coupled to the output of the first multiplexer, and an output coupled to the register file.

2. The apparatus of claim 1, further comprising:

a barrel shifter (40) having an input coupled to the output of the summing circuit;

an adder (41) having an input coupled to an output of the barrel shifter; and

a second multiplexer (42) having a first input coupled to the output of the summing circuit and a second input coupled to an output of the adder.

3. The apparatus of claim 2, further comprising:

a third multiplexer (26) having a first input coupled to the output of the second multiplexer (42) and a second input coupled to the register file (12) for receiving a fifth (A) chaining variable; and

a fourth multiplexer (28) having a first input coupled to the output of the second multiplexer and a second input coupled to the register file (12) for receiving the third (D) chaining variable.

4. The apparatus of claim 3, wherein the second multiplexer and the fourth multiplexer receive a signal that transfers a summed value from the output of the summing

circuit to the register file when the message digest hardware accelerator is processing an SHA-1 hash algorithm.

5. The apparatus of claim 3, wherein the second multiplexer and the third multiplexer receive a signal that transfers a summed value from the output of the barrel shifter to the register file when the message digest hardware accelerator is processing an MD5 hash algorithm.

6. The apparatus of claim 3, further comprising:
a first shift circuit (16) having an input coupled to the register file for receiving the first (B) chaining variable; and
a fifth multiplexer (14) having a first input coupled to an output of the first shift circuit, a second input coupled to the input of the first shift circuit and an output coupled to the register file for providing the second chaining variable.

7. The apparatus of claim 6, further comprising:
a second shift circuit (18) having an input coupled to the register file for receiving the fifth (A) chaining variable; and
a sixth multiplexer (20) having a first input coupled to an output of the second shift circuit, a second input coupled to the input of the second shift circuit and an output coupled to another input of the summing circuit.

8. A circuit for generating hash values in a first hash mode and a second hash mode, comprising:
a storage circuit (34, 36);
a register array (32) having registers for storing a message and an output for providing a round dependent data value (Wt);
a register file (12) for storing first (B), second (C), third (D), fourth (E) and fifth (A) chaining variables; and
an adder (30) having a first input coupled for receiving a first set of constant values stored in the storage circuit for the first hash mode and a second set of constant values for

the second hash mode, a second input coupled to the output of the register array, a third input coupled for receiving the fifth (A) chaining variable in the second hash mode and a shifted fifth chaining variable in the first hash mode, a fourth input coupled for receiving a logical function in accordance with the first, second and third chaining variables, and a fifth input coupled for receiving the fourth chaining variable in the second hash mode and a zero value in the first hash mode.

14. An apparatus integrated to provide a hash value of a variable length message in accordance with a first algorithm and a second algorithm, comprising:
- a register file (12) having five registers preset to a first group of values for the first algorithm and to a second group of values for the second algorithm, the register file storing first (B), second (C), third (D), fourth (E) and fifth (A) chaining variables;
 - a function circuit (22) receiving first, second and third chaining variables and generating a first logical data value for the first algorithm and a second logical data value for the second algorithm;
 - a storage element (34, 36) for supplying a first set of constant values for the first algorithm and a second set of constant values for the second algorithm; and
 - a summing circuit (30) having a first input coupled to the output of the function circuit (22) and a second input coupled to the storage element for receiving one of the first and second sets of constant values.

15. The apparatus of claim 14, further including a register array (32) having a decoder circuit (120) and a plurality of registers for selecting a data word stored in one of the plurality of registers and supplying the data word to an output of the register array when computing the first algorithm.

16. The apparatus of claim 15, wherein the register array further includes:
- an exclusive-OR (116) coupled for simultaneously receiving first, second, third and fourth data words stored in the plurality of registers; and

a rotate block (118) having an input coupled to an output of the exclusive-OR and supplying a one bit left circular shift of the data generated by the exclusive-OR to one of the registers in the plurality of registers.

17. The apparatus of claim 15, wherein an output of the register array is supplied from a word wise circular queue when computing the second algorithm.
18. The apparatus of claim 14, wherein the first algorithm is an MD5 algorithm and the second algorithm is an SHA-1 algorithm.

Evidence Appendix

No evidence is submitted in this appendix

Related proceedings Appendix

There are no decisions under this appendix.